Remarks:

This amendment adds claims 32-40 to the above-referenced application. These claims are directed to the same invention as was the subject of prior claims 10, 17 and 19-21 in this application. The Examiner had previously rejected claims of this application over U.S. Patent No. 5,905,993 to Shinohara (the Shinohara patent). Applicant submits that claims 32-40 distinguish over the Shinohara patent and the other prior art of record for the reasons discussed below.

The present application describes a method of controlling a flash memory system that efficiently generates a logical address/physical address translation table stored in the RAM of the flash memory system. According to the present application, when generating the translation table, the method may group two or more physical memory blocks into a physical block area for each corresponding logical block. The address stored in the RAM is inadequate to completely locate the physical block. Rather, the address stored in the RAM specifies the target physical block area and searching identifies which of the blocks stored in the area is correct. Consequently, the described method requires a smaller RAM in the memory card to store the translation table, as compared to the conventional method such as used by the admitted prior art.

FIG. 34 illustrates one embodiment of the present invention where two physical blocks are grouped within a physical block area. In FIG. 34, the logical address/physical address translation table contains the mapping information between the logical blocks and the physical blocks areas. To correctly relate a physical block with a corresponding logical block, a physical block area is first located by looking into the translation table containing the logical block address. After locating the physical block area, the redundant divisions of the two physical blocks associated with the physical block area are searched to determine which physical block really corresponds to the designated logical block. Accordingly, the presently described method can accurately map the physical blocks with the logical blocks by the translation table. The described method, therefore, effectively reduces the size needed for the RAM to store the translation table.

Claim 32 distinguishes over the Shinohara patent by reciting:

> "wherein the physical block of the non-volatile memory has a data storage capacity equal to or larger than a storage capacity of a logical block; and

seeking a physical block by converting a requested logical block address to a physical block area address according to the translation table and then determining which physical block within the physical block area corresponds to the requested logical block address."

The Shinohara patent does not meet these limitations. The Shinohara patent describes a flash memory system that addresses a flash memory with cylinder number, head number and sector number information. The Shinohara memory converts this information into a logical block address and a sector address and then converts the logical block address portion of the address to a physical block address portion. Both this physical block address portion and the sector number information are used to address the data within the Shinohara patent's non-volatile memory. See Shinohara patent, col. 2, line 66 to col. 3, line 8 ("accessing the flash memory on the basis of the physical block address and the sector address.").

Claim 32 states that the claimed memory system uses a physical block capacity equal to or larger than the logical block. Consequently, the sectors of the Shinohara patent cannot be considered the claimed logical blocks, since many sectors are provided to store the information of on logical block in the Shinohara patent. See Shinohara patent, FIG. 3, col. 4, lines 59-67 and equation (2). Consequently, claim 32 and its dependent claims 32-37 distinguish over the art of record and are in condition for allowance.

Claim 38 distinguishes over the Shinohara patent and other references of record by reciting,

"wherein the table includes at least one logical block address entry that maps to an address within the cell array corresponding to two or more physical blocks and wherein the storage regions of the two or more physical blocks include two or more corresponding logical block addresses and one of the corresponding logical block addresses is the logical block address of the at least one logical block address entry."

As shown in FIG. 2 of the Shinohara patent, the Shinohara patent's system provides one to one mapping between logical block addresses and physical block addresses. There is no suggestion in the Shinohara patent of storing logical block address information within the physical blocks of

memory. As such, claim 38 and its dependent claims 39-40 distinguish over the prior art of record and are in condition for allowance.

In view of the foregoing, it is respectfully submitted that the application is in condition for allowance. Reexamination and reconsideration of the application, as amended, are requested.

If for any reason the Examiner finds the application other than in condition for allowance, the Examiner is requested to call the undersigned attorney at the Los Angeles, California telephone number (213) 337-6700 to discuss the steps necessary for placing the application in condition for allowance.

If there are any fees due in connection with the filing of this response, please charge the fees to our Deposit Account No. 50-1314.

Respectfully submitted,
HOGAN & HARTSON L.L.P.

Date: August 10, 2004

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